Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A ferroelectric capacitor comprising:

a bottom electrode which has a first region and a second region, wherein the first region has a first thickness and the second region has a second thickness greater than the first thickness, and wherein the second region is arranged at a central area of the bottom electrode and the first region is arranged at a peripheral area of the bottom electrode;

a dielectric layer formed on the first region of the bottom electrode;

a ferroelectric layer formed on the dielectric layer and on the second region of the bottom electrode; and

a top electrode formed on the ferroelectric layer,

wherein the dielectric layer is sandwiched between the first region of the bottom electrode and the ferroelectric layer, [[and]]

wherein a side surface of the first region of the bottom electrode, a side surface of the dielectric layer, a side surface of the ferroelectric layer and a side surface of the top electrode are aligned, and

wherein a distance between the bottom electrode and the top electrode at the

first region is greater than a distance between the bottom electrode and the top electrode at the second region.

Claim 2 (Original): The ferroelectric capacitor of claim 1, wherein the ferroelectric layer includes a damaged area which is formed on the dielectric layer.

Claim 3 (Previously Presented): The ferroelectric capacitor of claim 1, wherein the bottom electrode comprises the first region and the second region as a single unitary electrode.

Claim 4 (Previously Presented): The ferroelectric capacitor of claim 1, wherein a top surface of the dielectric layer is substantially coplanar and aligned with a top surface of the second region.

Claim 5 (Canceled)

Claim 6 (Original): The ferroelectric capacitor of claim 1, wherein the bottom electrode and the top electrode are made of an oxidation resistance metal or a conductive metal oxide.

Claim 7 (Previously Presented): The ferroelectric capacitor of claim 8, wherein the

upper layer of the second region of the bottom electrode is made of a material different than the first region and the lower layer of the second region of the bottom electrode.

Claim 8 (Previously Presented): The ferroelectric capacitor of claim 1, wherein the second region of the bottom electrode includes a lower layer and an upper layer.

Claim 9 (Previously Presented): The ferroelectric capacitor of claim 7, wherein the upper layer of the second region of the bottom electrode is made of platinum.

Claim 10 (Previously Presented): A ferroelectric capacitor comprising:

a bottom electrode having a step area;

a top electrode;

a ferroelectric layer formed between the bottom electrode and the top electrode; and

a dielectric spacer formed between the bottom electrode and the top electrode,

wherein a distance between the bottom electrode and the top electrode at the step area is greater than a distance between the bottom electrode and the top electrode at a central area of the ferroelectric capacitor, and

wherein the dielectric spacer decreases an electric field strength at the step area of the bottom electrode.

Claim 11 (Previously Presented): The ferroelectric capacitor of claim 10, wherein the bottom electrode includes a projecting portion arranged at a central area of the bottom electrode, and wherein the dielectric spacer is arranged around the projecting portion on the step area.

Claim 12 (Canceled)

Claim 13 (Original): The ferroelectric capacitor of claim 10, wherein a side surface of the bottom electrode, a side surface of the ferroelectric layer, a side surface of the dielectric spacer and a side surface of the top electrode are aligned.

Claim 14 (Currently Amended): A ferroelectric capacitor comprising:

a first electrode which has a plate portion and a projecting portion, wherein the projecting portion is arranged on a central area of the plate portion;

a spacer layer formed on a peripheral area of the first electrode and arranged around the projecting portion of the first electrode;

a ferroelectric layer formed on the spacer layer and on the projecting portion; and

a second electrode formed on the ferroelectric layer,

wherein a side surface of the plate portion of the first electrode, a side surface of the ferroelectric layer and a side surface of the second electrode are aligned, and

wherein a distance between the plate portion of the first electrode and the

second electrode is greater than a distance between the projecting portion of the first electrode and the second electrode.

Claim 15 (Canceled)

Claim 16 (Currently Amended): A semiconductor device comprising:

a semiconductor substrate;

a switching transistor formed on the semiconductor substrate, the switching transistor having a source region, a drain region and a gate electrode;

an insulating layer formed on the semiconductor substrate and the switching transistor;

a ferroelectric capacitor formed on a top surface of the insulating layer, the ferroelectric capacitor including

a bottom electrode formed on the insulating layer, the bottom electrode has a first region which has a first thickness and a second region which has a second thickness greater than the first thickness, wherein the second region is arranged at a central area of the bottom electrode and the first region is arranged at a peripheral area of the bottom electrode,

a dielectric layer formed on the first region of the bottom electrode,

a ferroelectric layer formed on the dielectric layer and on the second region, and

a top electrode formed on the ferroelectric layer,

wherein the dielectric layer is sandwiched between the first region of the bottom electrode and the ferroelectric layer, [[and]]

wherein a side surface of the first region of the bottom electrode, a side surface of the dielectric layer, a side surface of the ferroelectric layer and a side surface of the top electrode are aligned, and

wherein a distance between the bottom electrode and the top electrode at the first region is greater than a distance between the bottom electrode and the top electrode at the second region; and

a plug electrode which is embedded in the insulating layer, wherein the plug electrode connects the source region of the switching transistor to the bottom electrode of the ferroelectric capacitor.

Claim 17 (Original): The semiconductor device of claim 16, wherein the top surface of the insulating layer is formed substantially flat.

Claim 18 (Original): The semiconductor device of claim 16, wherein the ferroelectric capacitor is located over the source region of the switching transistor.

Claim 19 (Currently Amended): A semiconductor device comprising:

a semiconductor substrate;

a switching transistor formed on the semiconductor substrate, the switching transistor having a source region, a drain region and a gate electrode;

an insulating layer formed on the semiconductor substrate and the switching transistor;

a ferroelectric capacitor formed on a top surface of the insulating layer, the ferroelectric capacitor including

a bottom electrode formed on the insulating layer, the bottom electrode has a first region which has a first thickness and a second region which has a second thickness greater than the first thickness, wherein the second region is arranged at a central area of the bottom electrode and the first region is arranged at a peripheral area of the bottom electrode,

a dielectric layer formed on the first region of the bottom electrode,

a ferroelectric layer formed on the dielectric layer and on the second region, and

a top electrode formed on the ferroelectric layer,

wherein the dielectric layer is sandwiched between the first region of the bottom electrode and the ferroelectric layer, [[and]]

wherein a side surface of the first region of the bottom electrode, a side surface of the dielectric layer, a side surface of the ferroelectric layer and a side surface of the top electrode are aligned, and

wherein a distance between the bottom electrode and the top electrode

at the first region is greater than a distance between the bottom electrode and the top electrode at the second region; and

a wiring which connects the source region of the switching transistor to the top electrode of the ferroelectric capacitor.

Claim 20 (Original): The semiconductor device of claim 19, wherein the wiring includes a plug portion which extends from the source region of the switching transistor to the top surface of the insulating layer and a wiring portion which connects a top of the plug to the top electrode of the ferroelectric capacitor.

Claim 21 (New): A ferroelectric capacitor which includes a central area and a peripheral area, comprising:

a bottom electrode;

a top electrode;

a ferroelectric layer which is arranged between the top electrode and the bottom electrode; and

a dielectric layer which is arranged between the bottom electrode and the top electrode at a peripheral area of the ferroelectric capacitor, so that an electric field strength at the peripheral area of the ferroelectric capacitor is lower than an electric field strength at a central area of the ferroelectric capacitor,

wherein a side surface of the bottom electrode, a side surface of the dielectric

layer, a side surface of the ferroelectric layer and a side surface of the top electrode are aligned.

Claim 22 (New): The ferroelectric capacitor of claim 21, wherein a distance between the bottom electrode and the top electrode at the peripheral area is greater than a distance between the bottom electrode and the top electrode at the central area.